



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re the Application of: **HASHIMOTO, Hiroshi et al.**

Group Art Unit: **2714**

Serial No.: **09/960,399**

Examiner: **Howard Weiss**

Filed: **September 24, 2001**

P.T.O. Confirmation No.: 5652

For. **SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION PROCESS
THEREOF**

PETITION FOR EXTENSION OF TIME

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: May 18, 2004

Sir:

Applicants petition the Commissioner for Patents to extend the time for response to the Office Action dated November 19, 2003 for three months from February 19, 2004 to May 19, 2004.

Attached please find a check including the amount of \$950.00 to cover the cost of the extension for a large entity. In the event that any additional fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

05/19/2004 MGE BREM1 00000048 09960399

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950.00 OP

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP

George N. Stevens
Attorney for Applicant
Reg. No. 36,938

GNS/alw
Atty. Docket No. **011225**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930



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PATENT TRADEMARK OFFICE